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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Inventor(s): Craig Nemecek

Serial No.: 09/975,105 Group Art Unit:

Filed: 10/10/01 Examiner:

Title: HOST TO FPGA INTERFACE IN AN IN-CIRCUIT EMULATION SYSTEM

Form 1449

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
MB	A	6,144,327	11/07/00	Distinti et al.	341	126	08/12/97
MB	B	5,202,687	04/13/93	Distinti	341	158	06/12/91
	C						
	D						
	E						

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No
	F							
	G							
	H							

Related Pending US Patent Applications

Examiner Initial	No.	Docket Number, Title, Filing Date, Serial Number & Inventors
MB	I	CYPR-CD00182; "IN-SYSTEM CHIP EMULATOR ARCHITECTURE";10/10/01; 09/975,115; Snyder et al.
	J	CYPR-CD00183; "CAPTURING TEST/EMULATION AND ENABLING REAL-TIME DEBUGGING USING FPGA FOR IN-CIRCUIT EMULATION"; 10/10/01; 09/975,104; Snyder
	K	CYPR-CD00185; "EMULATOR CHIP-BOARD ARCHITECTURE AND INTERFACE"; 10/1/01; 09/975,030; Snyder et al.
	L	CYPR-CD00186" METHOD FOR BREAKING EXECUTION OF TEST CODE IN A DUT AND EMULATOR CHIP ESSENTIALLY SIMULTANEOUSLY AND HANDLING COMPLEX BREAKPOINT EVENTS"; 10/10/01; 09/975,338; Nemecek et al.

Examiner	Date Considered
MBroda	14 April 2005

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.